UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,672	08/28/2001	Toshiyuki Hirota	WN-2345	4866

466 7590 03/31/2003

YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

EXAMINER
LUU, THANH X

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,672	HIROTA, TOSHIYUKI	
	Examiner	Art Unit	
	Thanh X Luu	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *24 January 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to amendments and remarks filed January 24, 2003. Claims 1-14 are currently pending.

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on January 24, 2003 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Pocholle et al. (U.S. Patent 4,917,450).

Regarding claims 1-3 and 7, Pocholle et al. disclose (see Figure 2) a semiconductor device, comprising: a plurality of processing elements (CPU1-8); and a single switcher (RAM) that connects each of the plural processing elements to each other, wherein each of the plural processing elements includes a network interface (see

Figure 1; light emitting element and light receiving element) and is connected to the single switcher via the network interface. Pocholle et al. further disclose (see Figure 2) the plural processing elements are located around the single switcher (RAM) and the switcher is located at the center position of the semiconductor device. Pocholle et al. also disclose (see Figure 2) each of the plural processing elements has a function of the same hierarchical level (same processing function for each CPU).

Regarding claim 8, Pocholle et al. further disclose (see Figure 2) at least one of the plural processing elements (CPU1-8) and the single switcher (RAM) are located in a space where light is confined (under 25), and each of the at least one of the plural processing elements and the single switcher has a light emitting element and a light receiving element (see column 3, lines 3-9), thereby an optical communication is performed between the processing elements and the switcher.

4. Claims 1-5 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Levi et al. (U.S. Patent 5,148,504).

Regarding claims 1-5 and 7, Levi et al. disclose (see Figure 10) a semiconductor device, comprising: a plurality of processing elements (102, 103); and a single switcher (one instance of 108) that connects each of the plural processing elements to each other, wherein each of the plural processing elements includes a network interface (109, 110) and is connected to the switcher via the network interface. Levi et al. further disclose (see Figure 10) the processing elements are located around the switcher (108) and the switcher is located at the center position of the semiconductor device. In addition, Levi et al. disclose (see Figure 10) the processing elements and the switcher

are implemented in a single semiconductor chip (common substrate 101) or package. Levi et al. also disclose (see Figure 2) each of the processing elements has a function of the same hierarchical level (both ICs are high performance).

5. Claims 1, 6 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Carlson et al. (U.S. Patent 5,506,961).

Regarding claims 1, 6 and 13, Carlson et al. disclose (see Figures 1-3) a semiconductor device, comprising: a plurality of processing elements (IOPs); and a single switcher (105, 110, 115) that connects each of the plural processing elements to each other, wherein each of the plural processing elements includes a network interface (bus interface; see Figure 2) and is connected to the single switcher via the network interface. Carlson et al. also disclose (see Figures 1-3 and column 6, lines 10-14) one of the processing elements (server connection manager) and the switcher (112) are connected by peer-to-peer connection via at least one transmission line (bus). Carlson et al. further disclose (see Figure 2) each of the plural processing elements are only connected to the single switcher, through each respective network interface (bus interface).

6. Claims 1-5 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Hartmann (U.S. Patent 6,018,782).

Regarding claims 1-5, Hartmann discloses (see Figure 2) a semiconductor device, comprising: a plurality of processing elements (210); and a single switcher (240) that connects each of the plural processing elements to each other, wherein each of the plural processing elements includes a network interface (220) and is connected to the

single switcher via the network interface. Hartmann further discloses (see Figure 2) the plural processing elements are located around the single switcher (240) and the switcher is located at the center position of the semiconductor device. In addition, Hartmann discloses (see Figure 2) the processing elements and the switcher are implemented in a single semiconductor chip (100) or package.

Regarding claim 14, Hartmann discloses (see Figure 2) a device comprising: a plurality of peripheral input/output processing elements (any two of 210); a core processor (another of 210); and a single switcher (240) that connects each of the plural peripheral processing elements and the core processor to each other, wherein each of the plural peripheral processing elements and the core processor includes a network interface (210) and are connected to the single switcher via a respective network interface.

7. Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Bernet et al. (U.S. Patent 5,764,645).

Regarding claim 14, Bernet et al. disclose (see Figures 2 and 3) a device comprising: a plurality of peripheral input/output processing elements (any two of 50); a core processor (another of 50); and a single switcher (54) that connects each of the plural peripheral processing elements and the core processor to each other, wherein each of the plural peripheral processing elements and the core processor includes a network interface (53; see Figure 3) and are connected to the single switcher via a respective network interface.

8. Claims 1 and 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshimura et al. (U.S. Patent 5,506,961).

Regarding claims 1 and 9-12, Yoshimura et al. disclose (see Figure 1) a semiconductor device, comprising: a plurality of processing elements (1a, 1c, 1d); and a single switcher (26b) that connects the each of the processing elements to each other, wherein each of the plural processing elements includes a network interface (fibers 24) and is connected to the single switcher via the network interface. Yoshimura et al. also disclose (see Figure 21) a plurality of semiconductor chips (20) each of which includes the plurality of processing elements and the single switcher; and at least one inter-switcher (26c of Figure 1; included in each element 20) which connects the semiconductor chips to each other. Yoshimura et al. further disclose (see Figure 21) the plurality of semiconductor chips (20) and the inter-switcher are implemented two-dimensionally. In addition, Yoshimura et al. disclose (see Figures 1 and 21) the inter-switcher (26c) is located in one of the plurality of semiconductor chips and the semiconductor chips are implemented three-dimensionally (the chips have a width, depth and height). Further, since the switcher and the inter-switcher switches signals between circuits, Yoshimura et al. implements a circuit switching.

9. Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Mendelson et al. (U.S. Patent 6,343,083).

Regarding claim 14, Mendelson et al. disclose (see Figure 2) a device comprising: a plurality of peripheral input/output processing elements (PCs 218, 229); a core processor (236); and a single switcher (250, 214) that connects each of the plural

peripheral processing elements and the core processor to each other, wherein each of the plural peripheral processing elements and the core processor includes a network interface (ATM endpoints 242, 222, 227) and are connected to the single switcher via a respective network interface.

Response to Arguments

10. Applicant's arguments filed January 24, 2003 have been fully considered but they are not persuasive.

Regarding claims 1-3, 7 and 8, Applicant asserts that Pocholle et al. do not disclose that each of the processing elements communicates with each other. However, such language is not found in the claims. The claims simply state the elements connect to each other. As set forth above, Pocholle et al. do disclose the claimed invention in which the single switcher connects each of the processing elements to each other.

Regarding claims 1-5 and 7, Applicant asserts that Levi et al. do not disclose a single switcher. However, the claims use "comprising" language, which is open-ended. Thus, a prior art device can include more than a single switcher as long as a single switcher is connected as claimed. As set forth above, Levi et al. do disclose a single switcher (a single instance of 108) as claimed.

Regarding claims 1 and 6, Applicant asserts that Carson et al. do not disclose the processing elements connected to a single switcher. Examiner has clarified that the switcher comprises elements 105, 110 and 115, taken together. Since the claim

language does not preclude the inclusion of a bus as being part of a switcher, the invention remains anticipated by Carson et al.

Regarding claims 1 and 9-12, Applicant asserts that Yoshimura et al. do not disclose a single switcher. Examiner has clarified that element 26b is the single switcher as claimed. Therefore, the reference of Yoshimura et al. does anticipate the invention.

Thus, as set forth above, this rejection is proper.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh X. Luu whose telephone number is (703) 305-0539. The examiner can normally be reached on Monday-Friday from 6:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta, can be reached on (703) 308-4852. The fax phone number for the organization where the application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

txl
March 21, 2003

Que T. Le
Primary Examiner